UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,012	11/17/2003	Natsuki Yokoyama		9741

24956 7590 09/07/2005

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
GARLAND, STEVEN R	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,012	YOKOYAMA ET AL.	
	Examiner	Art Unit	
	Steven R. Garland	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *164-175* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *164-169* is/are allowed.

6)☒ Claim(s) *170-175* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/274,308.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 164-175 are pending and claims 1-163 have been canceled.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 6/16/05 has been entered.

3. The disclosure is objected to because of the following informalities: the status of the parent applications mentioned on page 1 should be updated.

Appropriate correction is required.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 170 is rejected under 35 U.S.C. 102(e) as being anticipated by Nishida et al. 5,436,848 (cited by applicant) .

Nishida et al. teaches processing semiconductor wafers according to a predetermined schedule in which the schedule is based on the processing time of the

longest step. See col. 2, lines 18-68. All processing and movements are based on the time of the longest step so as to achieve synchronized processing and movement of the wafers. Nishida also shows the use of a plurality of processing apparatuses each having a chamber, (figure 1 elements 41-44) transporting means in the form of a robot with moving means which serves to transport the wafer between the apparatuses (inter-apparatus transporter) and to load and unload the wafers to and from the chambers (transporting means). See the figures and col. 1, lines 38 to col. 3, line 4. Note figure 1 shows the use of chambers.

Nishida also teaches using intervals of the predetermined unit time (seconds) that is shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the transporter. Col. 2, line 18-32.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 171-175 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishida et al. 5,436,848 (cited by applicant).

Nishida et al. teaches processing semiconductor wafers according to a predetermined schedule in which the schedule is based on the processing time of the longest step. See col. 2, lines 18-68. All processing and movements are based on the time of the longest step so as to achieve synchronized processing and movement of the wafers. Nishida also shows the use of a plurality of processing apparatuses each having a chamber, (figure 1 elements 41-44) transporting means in the form of a robot with moving means which serves to transport the wafer between the apparatuses (inter-apparatus transporter) and to load and unload the wafers to and from the chambers (transporting means). See the figures and col. 1, lines 38 to col. 3, line 4. Note figure 1 shows the use of chambers.

Nishida also teaches using intervals of the predetermined unit time (seconds) that is shorter than the longest required time for either processing in each of the processing apparatuses or for transporting by the transporter. Col. 2, line 18-32.

Nishida also teaches delaying at various locations to maintain synchronized operation. Col. 17, line 65 to col. 18, line 22, for example.

Nishida however fails to specifically state that a waiting time into or out of a processing apparatus is incorporated into the processing time or that such waiting times are intervals of the predetermined time interval (seconds).

It would have been obvious to one of ordinary skill in the art to modify Nishida to incorporate a waiting time into the processing time instead of a transport time so as to maintain a fixed transport time and ease in maintaining synchronized operation.

Further it would have been obvious to one of ordinary skill in the art to use an integer number of seconds for each of the transporting and processing operations for ease in calculations and determining various time periods.

9. Claims 164-169 are allowed.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven R. Garland whose telephone number is 571-272-3741. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SRG/

Steven R Garland
Examiner
Art Unit 2125

8/23/05

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100